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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/706,752	11/07/2000	Ramesh Padmanabhan	0023-0001	5989

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EXAMINER	
WANG, ALBERT C	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/706,752	PADMANABHAN ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-14 and 37-45* is/are allowed.

6)☒ Claim(s) *15-28* is/are rejected.

7)☒ Claim(s) *29-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12 July 2004 has been entered.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

3. Claims 15 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang, U.S. Patent No. 5,563,891.

As per claim 15, Wang discloses a system for reliably receiving data, comprising:

means for receiving data and an unreliable clock signal (Fig. 3, data of lower rate signal and recovered write clock; Col. 2, lines 10-21, clock from lower rate signal is unreliable);

means for writing the data to a memory using the unreliable clock signal (Fig. 3, writing to elastic buffer 620);

means for generating a reliable clock signal by turning on and off a local clock signal (Fig. 3, logic circuit 645 generates clock signal for multiplexer 650; Col. 3, lines 53-67, enable signal enables pulses of read clock to be outputted);

means for generating a data enable signal (Fig. 3, justification decision circuit 635 generates justification signal; Col. 3, lines 53-67, justification signal acts as an enable signal);

means for reading the data from the memory using the data enable signal and the local clock signal (Fig. 3, read-out of data of lower rate signal using gapped read clock based on justification signal and local oscillator signal).

means for recovering the data based on the reliable clock signal (Fig. 3, multiplexer 650 recovers read-out data based on clock signal received from logic circuit 645).

As per claim 28, Wang discloses a receiver, comprising:

a reliable clock generator configured to receive data and an unreliable clock signal (Fig. 3, write data of lower rate signal to elastic buffer using recovered write clock; Col. 2, lines 10-21, clock from lower rate signal is unreliable), generate a reliable clock signal from a constant clock signal (Fig. 3, logic circuit 645 generates clock signal for data pump 650 from local oscillator), generate a first enable signal (Fig. 3, justification decision circuit 635 generates justification signal; Col. 3, lines 53-67, justification signal acts as an enable signal), read the data from the memory using the first enable signal and the constant clock signal (Fig. 3, read-out of data of lower rate signal using gapped read clock based on justification signal and local oscillator signal), and output the data and the reliable clock signal (Fig. 3, data and clock provided to data pump 650).

a receiver component configured to receive that data and the reliable clock signal form the reliable clock generator and recover data based on the reliable clock signal (Fig. 3, data pump 650).

Claim Rejections - 35 USC § 103

4. Claims 16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, U.S. Patent No. 5,563,891, in view of Serack, U.S. Patent No. 5,111,485.

As per claim 16, Wang teaches a method for recovering data, comprising:

receiving data and an unreliable clock signal (Fig. 3, data of lower rate signal and recovered write clock; Col. 2, lines 10-21, clock from lower rate signal is unreliable);

writing the data to a memory using the unreliable clock signal (Fig. 3, writing to elastic buffer 620);

generating a gapped clock signal by turning on and off a constant local clock signal (Fig. 3, gapped read clock; Col. 3, lines 53-67, enable signal enables pulses of read clock to be outputted);

generating a data enable signal (Fig. 3, justification decision circuit 635 generates justification signal; Col. 3, lines 53-67, justification signal acts as an enable signal); and

reading the data from the memory using the data enable signal and the constant local clock signal (Fig. 3, read-out of data of lower rate signal using gapped read clock based on justification signal and local oscillator signal).

However, while Wang teaches providing logic circuits generate the gapped clock and data enable signals (Fig. 3, logic circuit 645 and justification decision circuit 135), Wang does not expressly describe these logic circuits as state machines. Serack teaches state machines that generate gapped clock and control signals (Col. 6, lines 43-68, state machine 30; Col. 7, lines 1-13, state machine 32). Serack further teaches that state machines comprise logic circuits (Col. 5, lines 48-54). At the time of the invention, it would have been obvious to one of ordinary skill in

the art to describe Wang's logic circuits as state machine. To do so would have been a matter of using different nomenclature.

As per claim 17, Wang teaches generating an address for writing the data into the memory (Fig. 3, write pointer 115; Col. 2, lines 35-46).

As per claim 18, Wang teaches the generating a gapped clock signal includes:

generating an enable signal having at least two states (Fig. 3, justification signal; Col. 3, lines 53-67); and

turning on and off the constant local clock signal based on the state of the enable signal to generate the gapped clock signal (Fig. 3, with logic circuit 645; Col. 3, lines 53-67).

As per claim 19, Wang teaches determining whether the memory contains data (Fig. 3, with comparison circuit 630).

As per claim 20, Wang teaches the determining includes:

comparing a write address used to access the memory to a read address used to access the memory to determine whether the memory contains data (Col. 3, lines 26-37).

As per claim 21, Wang teaches stopping the constant local clock signal when the memory contains no data (Col. 3, lines 39-52, when memory level is below a threshold, justification signal is low; Col. 3, lines 62-65, when justification signal is low, read clock is not enabled).

As per claim 22, Wang discloses the unreliable clock signal operates at a frequency lower than a frequency of the constant local clock signal (Col. 2, line 65-67, "the read clock is faster than the write clock"); and

wherein the generating a gapped clock signal and the generating a data enable signal include: compensating for underflow conditions in the memory by turning off the constant local

clock signal and disabling the data enable signal (Col. 4, lines 23-27, reduce or eliminate slips; Col. 3, lines 39-52, when memory level is below a threshold, justification signal is low; Col. 3, lines 53-67, when justification signal is low, read clock is not enabled).

5. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang/Serack as applied to claim 16 above, and further in view of Co et al., U.S. Patent No. 5,602,882 ("Co").

As per claim 23, Wang teaches the unreliable clock signal operates at a frequency higher than a frequency of the constant local clock signal (Col. 3, lines 1-5, "read clock is slower than the write clock"). Co teaches generating a data error when overflow conditions occur (Col. 2, lines 33-38). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Co's register to Wang's system in order to ensure the integrity of the system.

6. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang/Serack as applied to claim 16 above, and further in view of Mays et al., U.S. Patent No. 5,384,770 ("Mays").

As per claim 24, Wang teaches the read logic is configured to turn off the constant local clock signal when the write logic receives no unreliable clock signal (Fig. 4, when phase difference is below the threshold, justification signal is low, so that read clock is not enabled), but does not expressly teach starting a counter. Mays teaches starting a counter when no data is received (Col. 11, lines 37-51, timer 17 counts down when no character interrupt signal is received). In Wang when no data is received, no unreliable clock signal is recovered. At the time of the invention, it would have been obvious to one skilled in the art to apply Mays' starting

a time-out counter to Wang's system. A motivation for doing so would have been to limit delays due to waiting for data accumulation (Col. 4, lines 20-33).

As per claim 25, Mays teaches determining write logic has received data before the counter reaches a predetermined count (Col. 11, lines 37-51, character interrupt signal is received before timer 17 reaches zero).

As per claims 26 and 27, Mays teaches determining that the counter has reached a predetermined count (Col. 11, lines 37-51, "timer 17 counts down from a predetermined initial value to zero and produces a time-out signal").

Allowable Subject Matter

7. Claims 1-14 and 37-45 are allowed.

8. Claims 29-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385 (571-272-3669 after moving in October). The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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September 28, 2004

THOMAS LEE
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